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AMENDED CLAIMS

This listing will replace all prior versions of the claims in the application.

1. (currently amended) A method for optimizing timing performance of an overall logic circuit where that overall logic circuit is implemented in a Field Programmable Gate Array (FPGA) with at least one programmable interconnect of the FPGA behaving in a way such that timing of logic signals routed by the programmable interconnect from a specific source to a specific load within the FPGA is affected negligibly by fanout to other loads connected to the same source, the method comprising the steps of:

a) synthesizing the overall logic for a first implementation in the FPGA, the synthesis including construction and a first placement of one or more logic functions on the FPGA,

b) analyzing ~~the~~ timing paths of the first implementation with the first placement,

c) determining one or more critical timing paths from analysis of the first implementation,

d) selecting as an object for improvement a specific critical timing path from the critical timing paths,

e) implementing in ~~another~~ a new way the critical logic in the selected specific critical timing path with the implementation of the critical logic performed with relative disregard as to the fanout of signals to other loads in the overall logic circuit and with the placement of logic functions in the ~~chosen~~ selected specific critical path designed primarily to minimize the

interconnected routing distance of the signals contributing to that ~~chosen~~ selected specific critical path, such implementation being operatively substituted for the first placement and being a selection of new logic elements to implement the selected specific critical path, with said selection of new logic elements being a duplication of ~~the~~ logic elements utilized in the first placement but forming a second placement of the logic functions on the FPGA, those new logic elements of the second placement placed in a more optimal placement than the first placement for minimizing the interconnected routing distance of the ~~chosen~~ selected specific critical path.

2. (currently amended) The method of Claim 1 in which the implementation of the critical logic in a said new way in step e) is limited only to changes in the placement of the logic elements in the ~~chosen~~ selected specific critical path.

3. (currently amended) The method according to claim 1 further comprising:

~~a)~~ f) modifying the second placement of logic functions in the overall logic circuit to accommodate the changes in placement of the ~~chosen~~ selected specific critical path while maintaining approximately the new placement of the critical logic,

~~b)~~ g) repeating steps b) through e) of claim 1 where the last implementation and placement of the overall logic circuit from step e) ~~of claim 1~~ becomes

the basis for starting again with this last implementation becoming the base implementation.

4. (currently amended) The method of Claim 3 in which the implementation of the critical logic in a said new way in step e) is limited only to changes in the placement of the logic elements in the ~~chosen~~ selected specific critical path.

5. (currently amended) A method for optimizing overall timing performance of a logic circuit comprising:

a) implementing a logic circuit in an FPGA, wherein the FPGA behaves in a way such that the timing of logic signals routed from a specific source to a specific load within the FPGA is affected negligibly by fanout to other loads connected to the same source;

b) synthesizing a first arrangement of a plurality of logic elements in the FPGA to form one or more logic functions within the logic circuit, wherein each logic function has a first placement in the FPGA;

c) analyzing the timing path of each logic function in its first placement;

d) determining a critical timing path from the analysis of the first placements;

e) duplicating one or more of ~~the~~ said logic elements forming the logic function having the critical timing path;

f) placing the duplicated elements in a second placement in the FPGA which has a shorter critical timing path than the first placement for the logic function having the critical timing path.

6. (original) The method of claim 5 further comprising repeating steps c) through f) where the placement resultant from step f) becomes the timing path used in step c).